National Semiconductor

DM54S474/DM74S474 4096-Bit (512 × 8) TRI-STATE® PROM
DM54S475/DM74S475 4096-Bit (512 × 8) Open-Collector PROM

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

See page 5-36 of the Memory Applications Handbook for detailed programming information.

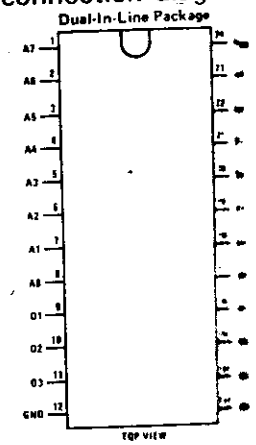
features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns
  Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

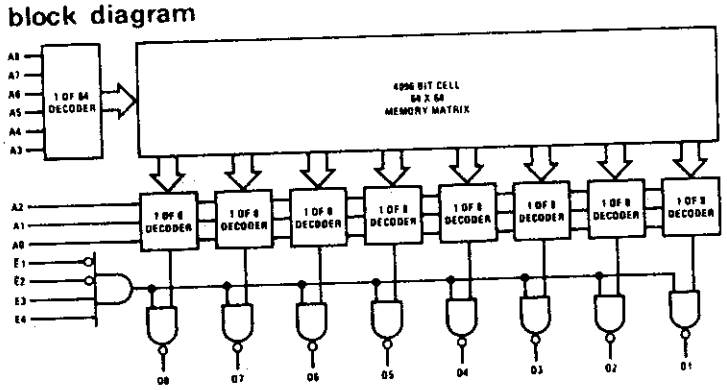
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S475		X	X		N, J
DM74S474		X		X	N, J
DM54S475	X		X		J
DM54S474	X			X	J

connection diagram

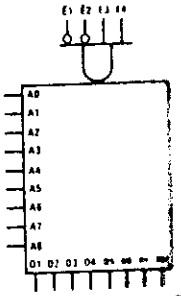
Dual-In-Line Package



block diagram



logic symbol



Order Number DM54S474J, DM54S475J, DM74S474J or DM74S475J
See NS Package J24A

Order Number DM74S474N or DM74S475N
See NS Package N24B

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S474, DM54S475	4.5	5.5	V
DM74S474, DM74S475	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S474, DM54S475	−55	+125	°C
DM74S474, DM74S475	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

	PARAMETER	CONDITIONS	DM54S474, DM54S475			DM74S474, DM74S475			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
IIL	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
IIH	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
VOL	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
VIL	Low Level Input Voltage				0.80			0.80	V
VIH	High Level Input Voltage		2.0			2.0			V
ICEX	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
VIC	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
CIN	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
COUT	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
ICC	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TATE PARAMETERS									
IOS	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
IOZ	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
VOH	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ectrical characteristics (With standard load)

	PARAMETER	CONDITIONS	DM54S474, DM54S475 5V ±10%; −55°C to +125°C			DM74S474, DM74S475 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	dress Access Time	*(Figure 1)*		40	75		40	65	ns
	able Access Time	*(Figure 2)*		20	40		20	35	ns
	able Recovery Time	*(Figure 2)*		20	40		20	35	ns

olute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device ted at these values.

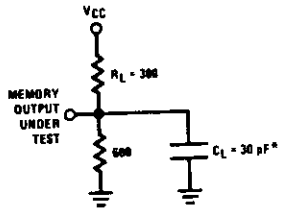
e limits do not apply during programming. For the programming ratings, refer to the programming instructions.

e limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

ng I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

asure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

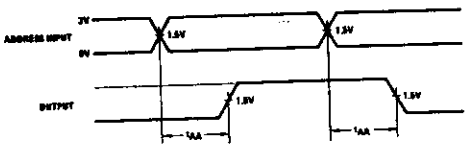


FIGURE 1. Address Access Time

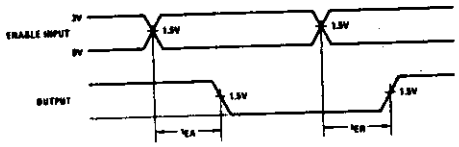
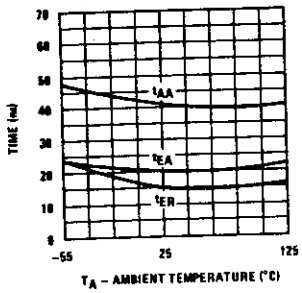


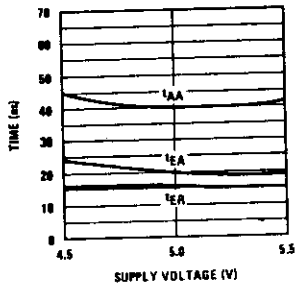
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

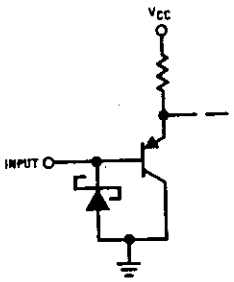


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

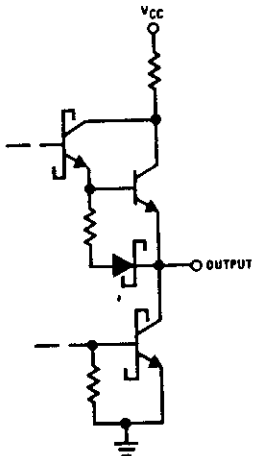


equivalent circuits

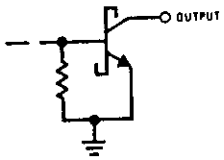
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7640A/41A

512 x 8 PROM

HM-7640A - Open Collector Outputs
HM-7641A - "Three State" Outputs

APRIL 1978

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIPS ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME — GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW INPUT LOADING

Description

The HM-7640A/41A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

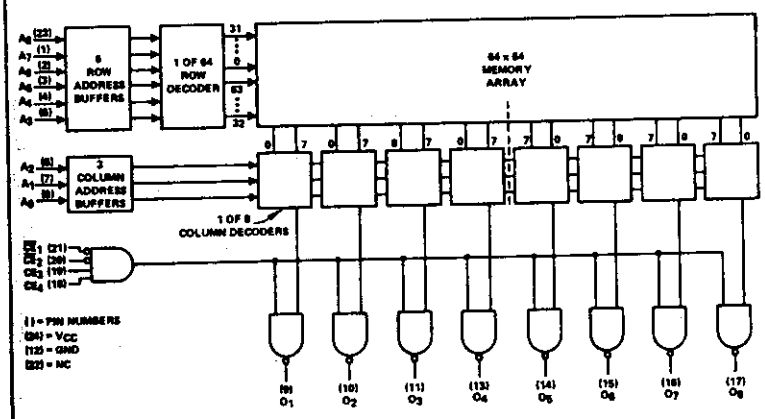
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7640A/41A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

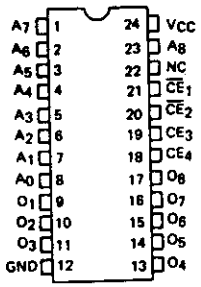
There are four chip enable inputs on the HM-7640A/41A where $\overline{CE}_1$, and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Functional Diagram

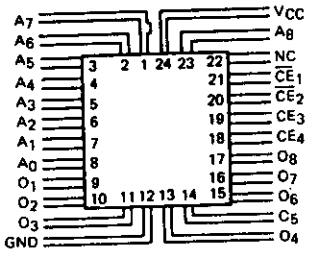


Pinouts

TOP VIEW – DIP



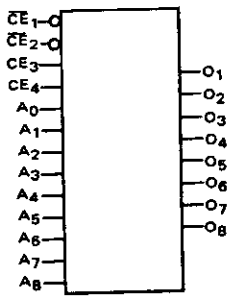
TOP VIEW – FLATPACK



PIN NAMES

A_0 - A_8	Address Inputs
O_1 - O_8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

Logic Symbol



Specifications HM-7640A/41A

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640A/41A-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640A/41A-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +12
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

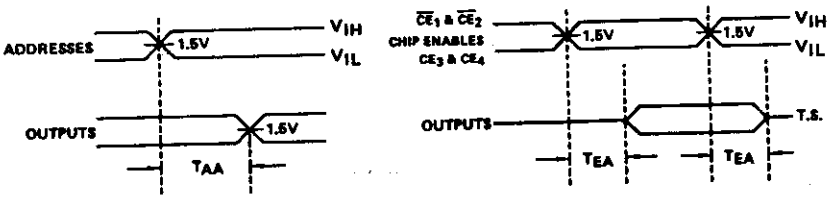
		HM-7640A/41A 5V ±5% 0°C to +75°C			HM-7640A/41A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

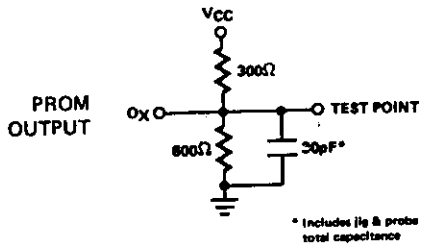
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

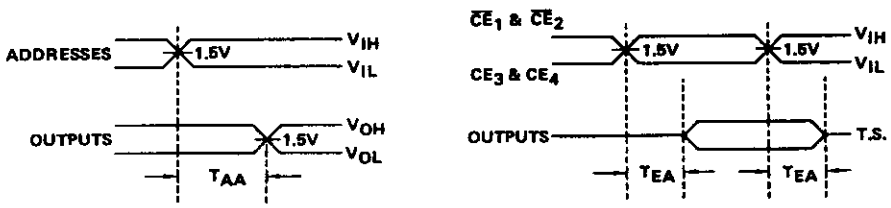
SWITCHING TIME DEFINITIONS



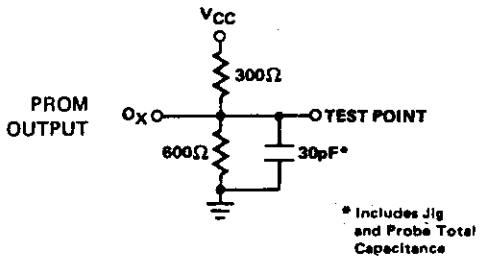
A.C. TEST LOAD



SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7642A/43A

1K x 4 PROM

HM-7642A - Open Collector Outputs
HM-7643A - "Three State" Outputs

MARCH 1978

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642A/43A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 1K words by 4 Bit/word format with open collector(HM-7642A) or "Three State" (HM-7643A) outputs. These PROM's are available in an 18—pin DIP (ceramic or epoxy) and an 18—pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

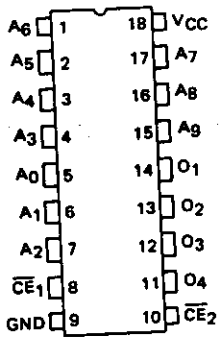
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7642A/43A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

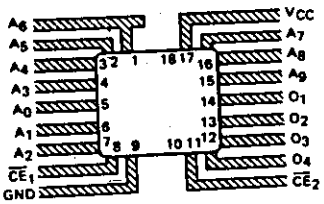
There are two chip enable inputs on the HM-7642A/43A. $\overline{CE}_1$ and $\overline{CE}_2$ Low enables the chip.

Pinout

TOP VIEW—DIP



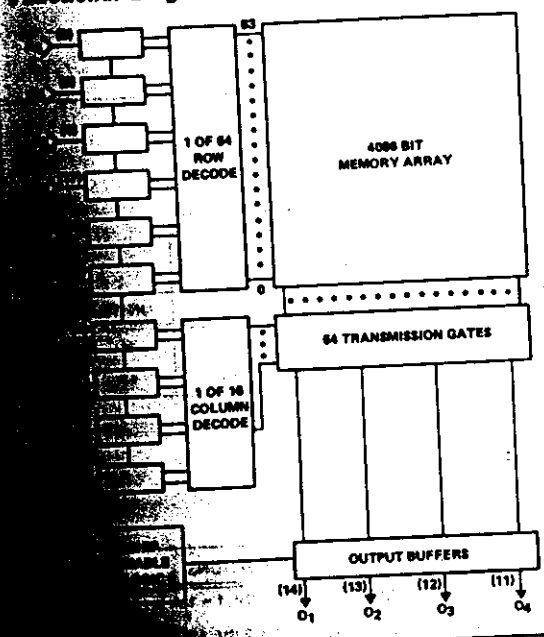
TOP VIEW—FLAT PACK



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2$	CHIP ENABLE INPUTS

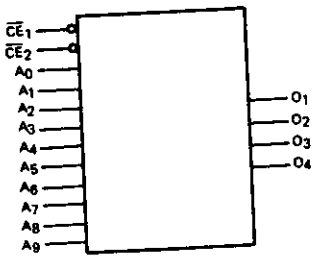
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_2, O_4 = (0 → 15)
O_1, O_3 = (15, 0 → 14)

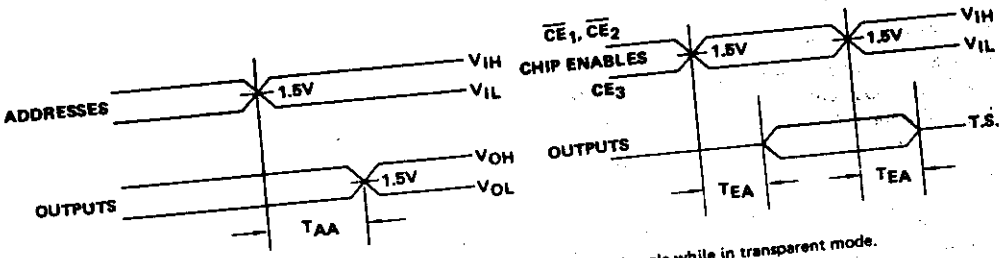
( ) = PIN NUMBERS
(18) = V_{CC}
(9) = GND

Logic Symbol



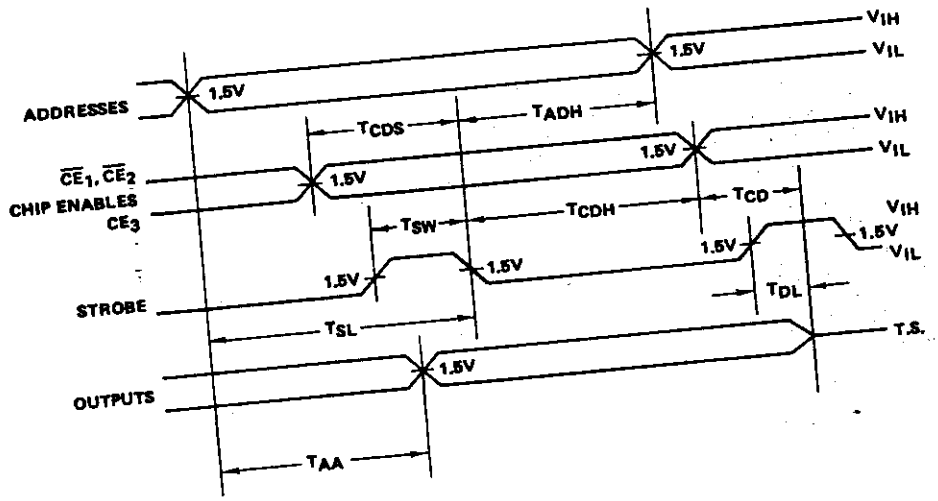
2

SWITCHING TIME DEFINITIONS (Transparent Mode)

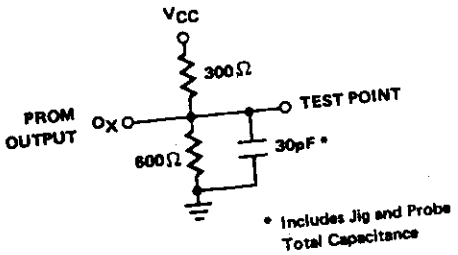


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD

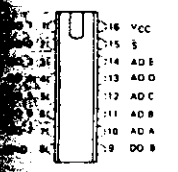


SERIES 54S/74S
PROGRAMMABLE READ-ONLY MEMORIES

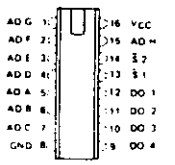
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

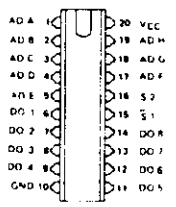
256 BITS (32 WORDS BY 8 BITS) 'S188, 'S288



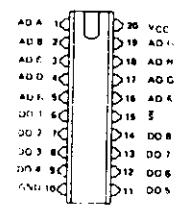
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



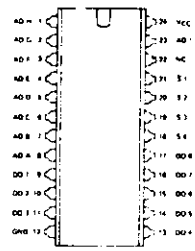
2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475



Pin assignments for all of these memories are the same for all packages

4

Description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program with a 100 microsecond pulse. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for ...ed memories as all are offered in dual-in-line packages having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET: ...elementary data may be ...ed at a later date.

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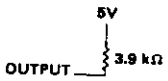
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

step-by-step programming procedure for the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output is 150 mA. This current flows from the programmer into the PROM output.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

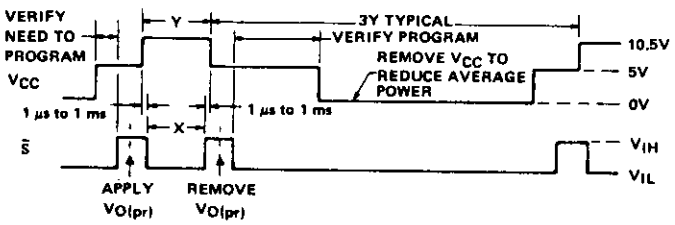


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

description (continued)

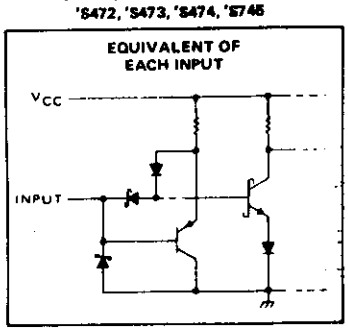
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

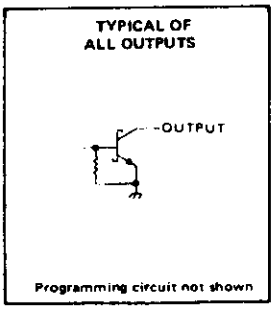
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

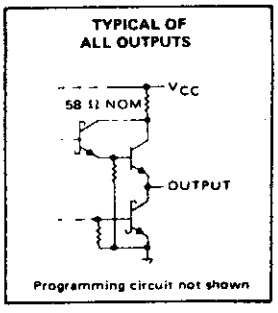
'S188, 'S287, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S745



'S188, 'S387, 'S470 S743, 'S475



'S287, 'S288, 'S471, 'S472, 'S474



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S' Circuits	−55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

recommended conditions for programming the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		98	100	10^3	μs
Programming duty cycle				25	35	%
Free-air temperature		0		55	°C

† Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 98 μs in duration.

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recommended operating conditions

PARAMETER		'S287, 'S471			'S288			'S472, 'S474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2			−2	mA
	Series 74S			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125♦	−55		125	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54S'			SN74S'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX		2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX				0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,				−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4		'S287		100	135		100	135	mA
				'S288		80	110		80	110	
				'S471		110	155		110	155	
				'S472, 'S474		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address			$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)			t_{PXZ} (ns) Disable time from high or low level			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{S})}$, 5 pF for t_{PXZ}, R_L = 300 Ω, See Figure 2, Page 13		42	75		15	40		12	40	ns
SN74S287			42	65		15	35		12	35	ns
SN54S288			25	50		12	30		8	30	ns
SN74S288			25	40		12	25		8	20	ns
SN54S471			50	80		20	40		15	35	ns
SN74S471			50	70		20	35		15	30	ns
SN54S472, SN54S474			55	85		20	45		15	40	ns
SN74S472, SN74S474			55	75		20	40		15	35	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
♦An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

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recommended operating conditions

PARAMETER		'S188			'S387, 'S470			'S473, 'S475			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				20			16			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125†	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S188		80	110	mA
			'S387		100	135	
			'S470		110	155	
			'S473; 'S475		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select (disable time)			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1, Page 13		25	50		12	30		12	30	ns
SN74S188			25	40		12	25		12	25	ns
SN54S387			42	75		15	40		15	40	ns
SN74S387			42	65		15	35		15	35	ns
SN54S470			50	80		20	40		15	35	ns
SN74S470			50	70		20	35		15	30	ns
SN54S473, SN54S475			55	85		20	45		15	40	ns
SN74S743, SN74S475			55	75		20	40		15	35	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

SN74S478

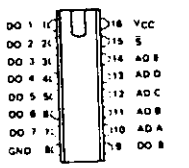
SCHOTTKY† PROM'S

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

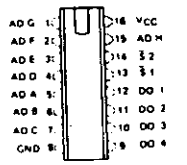
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
–55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

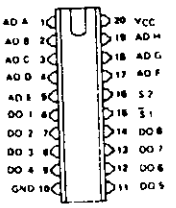
256 BITS (32 WORDS BY 8 BITS) 'S188, 'S288



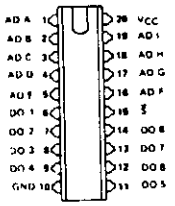
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



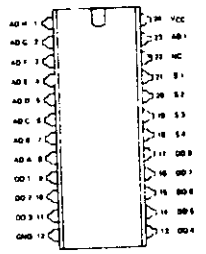
2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475



Pin assignments for all of these memories are the same for all packages.

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The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for fixed memories as all are offered in dual-in-line packages having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

4

description (continued)

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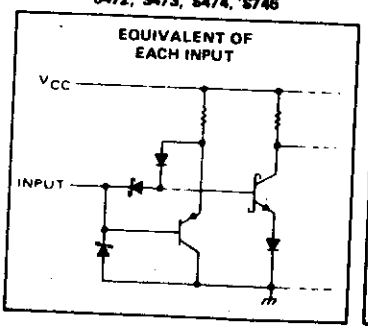
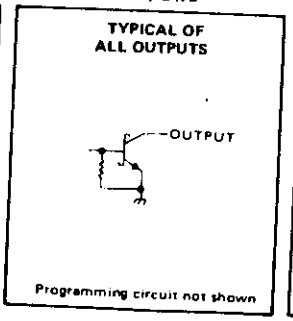
schematics of inputs and outputs

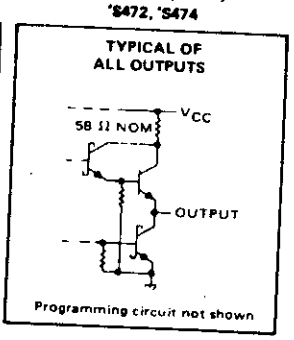
'S188, 'S287, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S746



'S188, 'S387, 'S470 S743, 'S475



'S287, 'S288, 'S471, 'S472, 'S474



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended conditions for programming the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
Input voltage	Program pulse	10	10.5	11†	V
	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		98	100	10³	μs
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

†Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 98 μs in duration.

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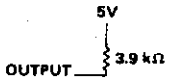
step-by-step programming procedure for the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output is 150 mA. This current flows from the programmer into the PROM output.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

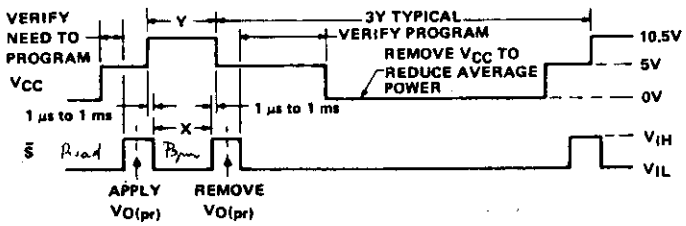


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

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Bipolar PROM Cross Reference Guide

SIZE AND ORGANIZATION	OUTPUT	NATIONAL MIL/COM	AMD M = MIL C = COM	FAIRCHILD M = MIL C = COM	HARRIS 2 = MIL 5 = COM	INTEL M = MIL P = COM	INTERSIL M = MIL C = COM	M.M.I. MIL/COM –1 = SCHOTTKY	SIGNETICS S = MIL N = COM	T.I. MIL/COM
256-Bit (32 x 8) 16-Pin	OC	DM54S188/DM74S188	AM27S08		HM1-7602 HM1-8256		IM5600	5330/6330	8223 82S23	SN54188A/74188A SN54S188/74S188
	TS	DM54S288/DM74S288	AM27S09		HM1-7603		IM5610	5331/6331	82S123	SN54S288/74S288
1024-Bit (256 x 4) 16-Pin	OC	DM54S387/DM74S387	AM27S10	93417 93416	HM1-7610 HM1-1024A	3601-1 3601	IM5603	5300/6300	82S126	SN54S387/74S387
	TS	DM54S287/DM74S287	AM27S11	93427 93426	HM1-7611 HM1-1024	3621	IM5623	5301/6301	82S129	SN54S287/74S287
2048-Bit (512 x 4) 16-Pin	OC	DM54S570/DM74S570		93436	HM1-7620	3602	IM5604	5305/6305	82S130	
	TS	DM54S571/DM74S571		93446	HM1-7621	3622	IM5624	5306/6306	82S131	
4096-Bit (512 x 8) 24-Pin	OC	DM54S475/DM74S475		93438	HM1-7640	3604	IM5605	5340/6340	82S140	SN54S475/74S475
	TS	DM54S474/DM74S474		93448	HM1-7641	3624	IM5625	5341/6341	82S141	SN54S474/74S474
4096-Bit (512 x 8) 20-Pin	OC	DM54S473/DM74S473						5348/6348		SN54S473/74S473
	TS	DM54S472/DM74S472						5349/6349		SN54S472/74S472
4096-Bit (1024 x 4) 18-Pin	OC	DM54S572/DM74S572*		93452	HM1-7642	3605		5352/6352	82S136	
	TS	DM54S573/DM74S573*		93453	HM1-7643	3625		5353/6353	82S137	

Note: All manufacturer's PROMs program differently.
*Future products

TOTAL BITS	PART NUMBER PROM	PART NUMBER ROM	ORGANIZATION		NUMBER OF PINS	TEMPERATURE RANGE	MAXIMUM ADDRESS ACCESS (t_{AA})	MAXIMUM SUPPLY CURRENT (I_{CC})
256	DM54S188		32 x 8	OC	16	–55°C to +125°C	45	110
	DM74S188		32 x 8	OC	16	0°C to +70°C	35	110
	DM54S288		32 x 8	TS	16	–55°C to +125°C	45	110
	DM74S288		32 x 8	TS	16	0°C to +70°C	35	110
1024	DM54S387	DM54S187	256 x 4	OC	16	–55°C to +125°C	60	130
	DM74S387	DM74S187	256 x 4	OC	16	0°C to +70°C	50	130
	DM54S287	DM75S97	256 x 4	TS	16	–55°C to +125°C	60	130
	DM74S287	DM85S97	256 x 4	TS	16	0°C to +70°C	50	130
2048	DM54S570	DM54S270	512 x 4	OC	16	–55°C to +125°C	65	130
	DM74S570	DM74S270	512 x 4	OC	16	0°C to +70°C	55	130
	DM54S571	DM54S370	512 x 4	TS	16	–55°C to +125°C	65	130
	DM74S571	DM74S370	512 x 4	TS	16	0°C to +70°C	55	130
4096	DM54S572		1k x 4	OC	18	–55°C to +125°C	75	140
	DM74S572		1k x 4	OC	18	0°C to +70°C	60	140
	DM54S573		1k x 4	TS	18	–55°C to +125°C	75	140
	DM74S573		1k x 4	TS	18	0°C to +70°C	60	140
4096	DM54S475	DM77S95	512 x 8	OC	24	–55°C to +125°C	75	170
	DM74S475	DM87S95	512 x 8	OC	24	0°C to +70°C	65	170
	DM54S474	DM77S96	512 x 8	TS	24	–55°C to +125°C	75	170
	DM74S474	DM87S96	512 x 8	TS	24	0°C to +70°C	65	170
8192		DM75S29	1k x 8	OC	24	–55°C to +125°C	90	160
		DM85S29	1k x 8	OC	24	0°C to +70°C	70	160
		DM75S28	1k x 8	TS	24	–55°C to +125°C	90	160

SERIES 24 AND 28 STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

BULLETIN NO. DL-S 12730, SEPTEMBER 1979

- New, Expanded Family of Standard, Low Power, Power Down, And Registered PROMs
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Full-Family-Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs for Reduced Loading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:
  Microprogramming/Firm Ware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

STANDARD PROMS

TYPE NUMBER		OUTPUT CONFIGURATION[♦]	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP24S10 (J, N)†		▽	1024 Bits (256W X 4B)	35 ns	20 ns	375 mW
TBP24SA10 (J, N)†		Ω				
TBP28S42 (J, N)†		▽	4096 Bits (512W X 8B)	35 ns	15 ns	800 mW
TBP28S45 (J, N)†		▽				
TBP24S41 (J, N)[Δ]	SN74S476 (J, N)	▽	4096 Bits (1024W X 4B)	40 ns	20 ns	475 mW
TBP24SA41 (J, N)[Δ]	SN74S477 (J, N)	Ω				
TBP24S81 (J, N)	SN74S474 (J, N)	▽	8192 Bits (2048W X 4B)	45 ns	20 ns	625 mW
TBP24SA81 (J, N)	SN74S475 (J, N)	Ω				
TBP28S86 (J, N)	SN74S478 (J, N)	▽	8192 Bits (1024W X 8B)	45 ns	20 ns	625 mW
TBP28SA86 (J, N)	SN74S479 (J, N)	Ω				
TBP28S2708 (J, N)	SN74S2708 (J, N)	▽				
TBP28S85 (J, N)†		▽		35 ns	15 ns	580 mW
TBP28S166 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	15 ns	640 mW

LOW POWER PROMS

TYPE NUMBER		OUTPUT CONFIGURATION[♦]	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28L22 (J, N)†		▽	2048 Bits (256W X 8B)	45 ns	35 ns	300 mW
TBP28L42 (J, N)†		▽	4096 Bits (512W X 8B)	60 ns	30 ns	250 mW
TBP28L45 (J, N)†		▽				
TBP28L86 (J, N)[Δ]	SN74LS478 (J, N)	▽	8192 Bits (1024W X 8B)	80 ns	35 ns	350 mW
TBP28L85 (J, N)†		▽		65 ns	30 ns	275 mW
TBP28L166 (J, N)†		▽	16,384 Bits (2048W X 8B)	65 ns	30 ns	250 mW

† NOTE – Electrical parameters for these devices are design goals only.

[Δ] NOTE – These devices available as full-temperature-range and as high-rel processed devices (use suffix MJ or NJ).

[♦] Ω = open collector, ▽ = three state.

5

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

POWER DOWN PROMS

TYPE NUMBER		OUTPUT CONFIGURATION†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28P42 (J, N)†		▽	4096 Bits (512W X 8B)	35 ns	35 ns	600/60 mW
TBP28P45 (J, N)†		▽				
TBP28P85 (J, N)†		▽	8291 Bits (1024W X 8B)	35 ns	35 ns	550/60 mW
TBP28P165 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	35 ns	500/75 mW

REGISTERED PROMS

TYPE NUMBER		OUTPUT CONFIGURATION†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				CLOCK TO OUTPUT	ADDRESS SET UP TIME	POWER DISSIPATION
TBP 28R45 (J, N)†		▽	4096 Bits (512W X 8B)	20 ns	20 ns	550 mW
TBP28R85 (J, N)†		▽	8192 Bits (1024W X 8B)			600 mW
TBP28R165 (J, N)†		▽	16,384 Bits (2048W X 8B)			550 mW

†Electrical parameters for these devices are design goals only.
▽= three-state.

Description

The new 24 and 28 Series of monolithic TTL programmable read-only memories (PROMs) feature an expanded selection of standard, low-power, power-down, and registered PROMs. This expanded PROM family provides the system designer with considerable flexibility in upgrading existing designs or optimizing new designs. Featuring proven titanium-tungsten (Ti-W) fuse links with low-current MOS-compatible p-n-p inputs, all family members utilize a common programming technique designed to program each link with a 100-microsecond pulse.

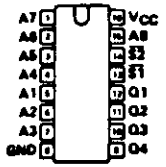
The new 4096-bit and 8192-bit PROMs are offered in 24-pin 300-mil-wide packages, greatly improving system density for large PROM arrays. For systems requiring even higher levels of complexity and density, the 16,384-bit PROMs provide twice the bit density of the 8192-bit PROMs in 24-pin 600-mil-wide packages. All PROMs are supplied with a logic-high output level stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) (S or $\overline{S}$) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off. On power-down PROMs, active level(s) at the chip-enable input(s) (E or $\overline{E}$) power up the device and enables all of the outputs. An inactive level at any chip-enable input causes all the outputs to be off and the PROM to be in a reduced-power standby mode.

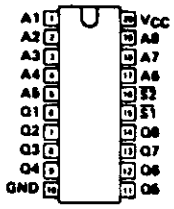
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

PIN ASSIGNMENTS (TOP VIEWS)

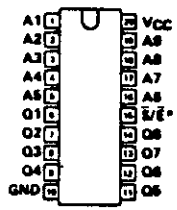
TBP24S10, TBP24SA10
1024 BITS
(256 WORDS BY 4 BITS)



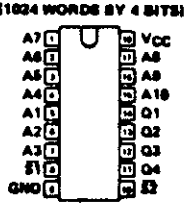
TBP28L22
2048 BITS
(256 WORDS BY 8 BITS)



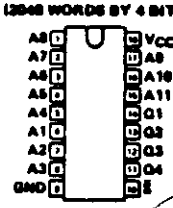
TBP28S42*, TBP28L42,
TBP28P42 4096 BITS
(512 WORDS BY 8 BITS)



TBP34S41, TBP24SA41
4096 BITS
(1024 WORDS BY 4 BITS)

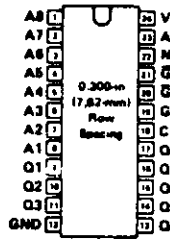


TBP24S81, TBP24SA81
8192 BITS
(2048 WORDS BY 4 BITS)

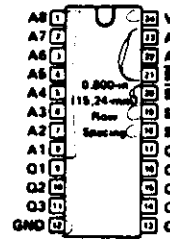


TBP28S45, TBP28L45, TBP28P45*
4096 BITS
(512 WORDS BY 8 BITS)

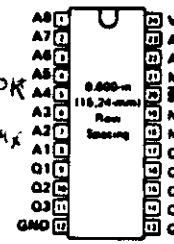
TBP28R45
4096 BITS
(512 WORDS BY 8 BITS)



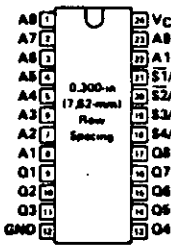
TBP28S86, TBP28SA86, TBP28L86
8192 BITS
(1024 WORDS BY 8 BITS)



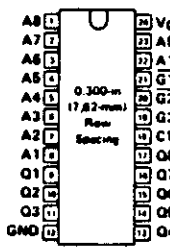
TBP28S2708
8192 BITS
(1024 WORDS BY 8 BITS)



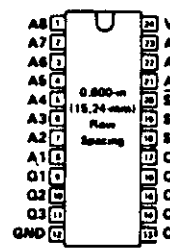
TBP28S85, TBP28L85, TBP28P85*
8192 BITS
(1024 WORDS BY 8 BITS)



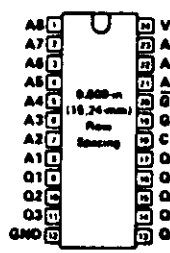
TBP28R85
8192 BITS
(1024 WORDS BY 8 BITS)



TBP28S166, TBP28L166, TBP28P166*
16,384 BITS
(2048 WORDS BY 8 BITS)



TBP28R166
16,384 BITS
(2048 WORDS BY 8 BITS)



NC = No internal connection

* For those pins having dual designations, the designation to the right of the virgule (/) applies only to the type number(s) immediately followed by an asterisk (*) above the pinout drawing.

tandard PROMs

The standard PROM members of Series 24 and 28 offer the highest performance for applications requiring the uncompromised speed of Schottky technology. The fast chip-select access times allow additional decoding delays to occur without degrading speed performance.

ow-power PROMs

To upgrade systems utilizing MOS EPROMs or MOS PROMs, the low-power PROM family offers the increased output drive and speed performance of bipolar technology and the reduced power dissipation necessary to implement effective upgrades. Additionally, low-power PROMs offer substantially reduced power dissipation over standard PROMs with minimal speed penalty.

ower-down PROMs

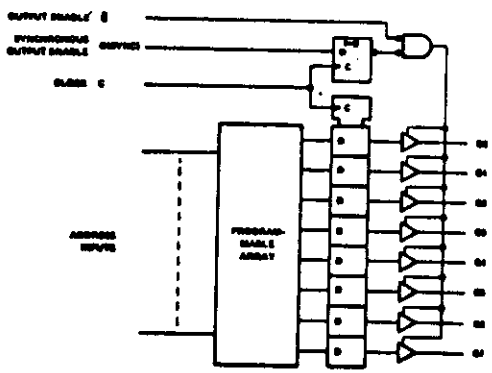
For power-sensitive systems requiring the speed performance of the standard PROM members as well as reduced system power dissipation, the power-down PROM members allow a 75% or better reduction in power dissipation when disabled while providing standard PROM speed performance when enabled. The power-down and power-up functions are sequenced to occur with the outputs at a high-impedance state. The enable (power-up) function provides adequate performance to allow power-up to occur during the normal read access time precluding any degradation in memory speed performance.

egistered PROMs

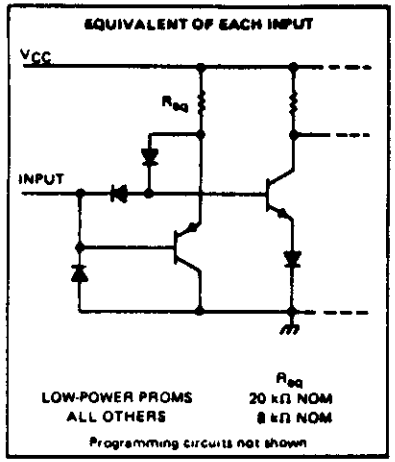
For microprogrammed pipelined systems the Series 24 and 28 registered PROM members offer the system designer reduced package count and improved system performance by incorporating the pipeline register onto the PROM chip. Available in 4096-bit, 8192-bit and 16,384-bit densities, all registered PROMs are provided with synchronous and asynchronous output controls (G and $\overline{G}$) allowing maximum flexibility in data bus control.

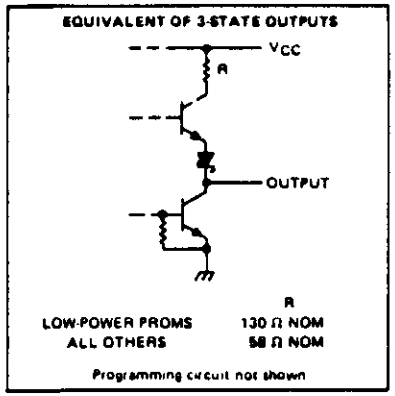
When power is first applied, the edge-triggered latch for the synchronous output control is cleared, and the O outputs are placed in a high-impedance state. To read data, the address is set up, the synchronous output enable, G(SYNC), is taken high, and a low-to-high transition on the clock (C) input causes the selected data to be stored in the registers. That same transition causes the outputs to be enabled if asynchronous output enable $\overline{G}$ is low. At this time the address may be changed and a new word addressed without affecting the register contents. If the synchronous output enable is low at the time of a low-to-high clock transition, the outputs will be disabled to the high-impedance state. They may be disabled at any time by taking output enable $\overline{G}$ high.

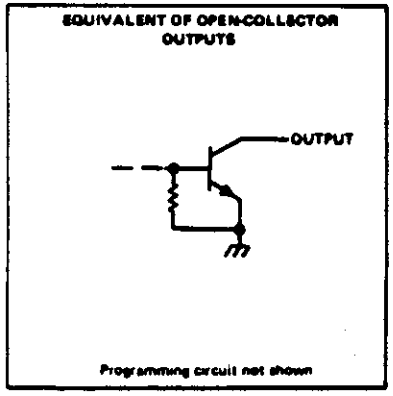
block diagram (positive logic)



schematics of inputs and outputs







5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Chip-select peak input voltage (S, S1, S2) (see Note 2)	11 V
Off-state output voltage	5.5 V
Off-state peak output voltage (see Note 2)	17.25 V
Operating free-air temperature range: Full-temperature-range circuits (MJ)	−55°C to 125°C
Commercial-temperature-range circuits (J, N)	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES 1. Voltage values are with respect to network ground terminal.
2. These ratings apply only under the conditions described in the programming procedure.

recommended operating conditions

PARAMETER		TBP28SA86			TBP24SA81, TBP24SA41			TBP24SA10*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}	MJ			12			16			16	mA
	J, N			12			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP24SA81 TBP28SA86			TBP24SA41			TBP24SA10*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50			50	µA
			V_O = 5.5 V			100			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	MJ			0.5			0.5			0.5	V
			J, N			0.5			0.5			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	µA
I_{CC}	Supply current	V_{CC} = MAX	MJ		125			95	140		75		mA
			J, N		125	175		95	140		75		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP24SA10*	MJ	C_L = 30 pF, See Page 1-14		35			20	40		15	40	ns
	J, N			35			20	30		15	30	
TBP24SA81				45	70		20	40		20	40	ns
TBP24SA41	MJ			40	75		20	40		20	40	ns
	J, N			40	60		20	30		20	30	
TBP28SA86				45	70		20	40		20	40	ns

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designates commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP24S10*			TBP28S86, TBP28S270S			TBP24S81, TBP24S41			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			12			16	mA
	J, N			16			12			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP24S10*			TBP24S81, TBP24S86, TBP28S270S			TBP24S41			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	µA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ					125	175		95	140	mA
			J, N		75			125	175		95	140	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP24S10*	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 300 Ω, See Page 1-14		35			20	35		15	35	ns
	J, N				35			20	40		15	30	
TBP24S81					45	70		20	40		20	40	ns
TBP24S41	MJ				40	75		20	40		20	40	ns
	J, N				40	60		20	30		20	30	
TBP28S86					45	70		20	40		20	40	ns
TBP28S270S													

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designates commercial-temperature-range circuits (formerly 74 Family).

mmended operating conditions

PARAMETER		TBP28S42*, TBP28S46*			TBP28S86*			TBP28S166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
ply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
h-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
w-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
rating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

trical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28S42*, TBP28S46*			TBP28S86*			TBP28S166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
	High-level input voltage			2			2			2			V
	Low-level input voltage					0.8			0.8			0.8	V
	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
	Supply current	V_{CC} = MAX	MJ		105			110			100		mA
			J, N		105			110			100		

conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
typical values are at V_{CC} = 5 V, T_A = 25°C.
e more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

hing characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
P28S42* P28S46*	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 300 Ω, See Page 1-14		35			15			12		ns
P28S86*				35			15			12		ns
P28S166*				35			15			12		ns

rical parameters for these devices are design goals only.

: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28L22*			TBP28L42*, TBP28L46*			TBP28L86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−1			−1			−1	mA
	J, N			−1.6			−1.6			−1.6	
Low-level output current, I_{OL}	MJ			8			8			4	mA
	J, N			8			8			8	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28L22*			TBP28L42* TBP28L42*			TBP28L86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−10		−100	−10		−100	−10		−100	mA
			J, N	−10		−100	−10		−100	−10		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ								80	100	mA
			J, N		60	86		80			80	100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28L22*	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 600 Ω, See Page 1-15		45			20			15		ns
	J, N				45			20			15		ns
TBP28L42* TBP28L46*					80			30			25		ns
TBP28L86	MJ				85	175		55	135		50	90	ns
	J, N				85	130		55	90		50	75	

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

mended operating conditions

PARAMETER		TBP28L86°			TBP28L166°			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
y voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	
level output current, I_{OH}	MJ			−1			−1	mA
	J, N			−1.6			−1.2	
level output current, I_{OL}	MJ			8			8	mA
	J, N			8			8	
ing free-air temperature range	MJ	−55		125	−55		125	°C
	J, N	0		70	0		70	

ical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TBP28L86°			TBP28L166°			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level input voltage			2			2			V
Low-level input voltage					0.8			0.8	V
Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5	V
Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50	µA
Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50	µA
Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	µA
Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	µA
Short-circuit output current§	V_{CC} = MAX	MJ	−10		−100	−10		−100	mA
		J, N	−10		−100	−10		−100	
Supply current	V_{CC} = MAX	MJ		55			50		mA
		J, N		55			50		

conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
typical values are at V_{CC} = 5 V, T_A = 25°C.
more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

hing characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(E)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
28L86°	C_L = 30 pF for $t_{a(A)}$ and $t_{a(E)}$. C_L = 5 pF for t_{PXZ}	R_L = 600 Ω, See Page 1-15		65			30			25		ns
28L166°				65			30			25		ns

rical parameters for these devices are design goals only.
: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28P42°, TBP28P45°			TBP28P86°			TBP28P166°			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28P42°, TBP28P45°			TBP28P86°			TBP28P166°			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	µA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	Power Up	V_{CC} = MAX		100			110			100		mA
		Power Down			12			12			15		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(E)}$ Access time from chip enable (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28P42°, TBP28P45°	C_L = 30 pF for $t_{a(A)}$ and $t_{a(E)}$. C_L = 5 pF for t_{PXZ}	R_L = 300 Ω, See Page 1-14		35			35			12		ns
TBP28P86°				35			35			12		ns
TBP28P166°				35			35			12		ns

†Electrical parameters for these devices are design goals only.

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

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recommended operating conditions

PARAMETER		TBP28R45*			TBP28R85*			TBP28R166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Clock pulse width high, $t_{w(CH)}$		20			20			20			ns
Clock pulse width low, $t_{w(CL)}$		20			20			20			ns
Address setup time, $t_{su(A)}$		20			20			20			ns
Chip select setup time, $t_{su(S)}$		0			0			0			ns
Address hold time, $t_{h(A)}$		0			0			0			ns
Chip select hold time, $t_{h(S)}$		5			5			5			ns
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28R45*			TBP28R85*			TBP28R166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	MJ			0.5			0.5			0.5	V
			J, N			0.5			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		110			120			110		mA
			J, N		110			120			110		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
¶ Electrical and switching parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

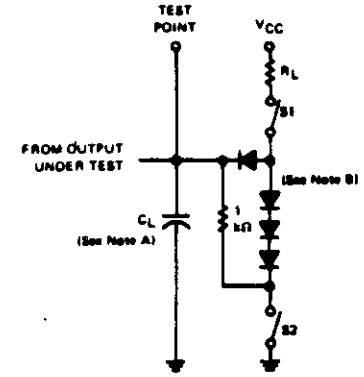
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

types TBP28R45*, TBP28R85*, TBP28R166*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{a(C)}$	Access time from clock	R_L = 300 Ω, C_L = 30 pF, See Figure 1			20	ns
$t_{PXZ(C)}$	Output disable time from clock				30	ns
$t_{PZX(C)}$	Output enable time from clock				30	ns
$t_{PXZ(G)}$	Output disable time from G				12	ns
$t_{PZX(G)}$	Output enable time from G				15	ns

* Electrical and switching parameters for these devices are design goals only.

PARAMETER MEASUREMENT INFORMATION



NOTES. A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

LOAD CIRCUIT

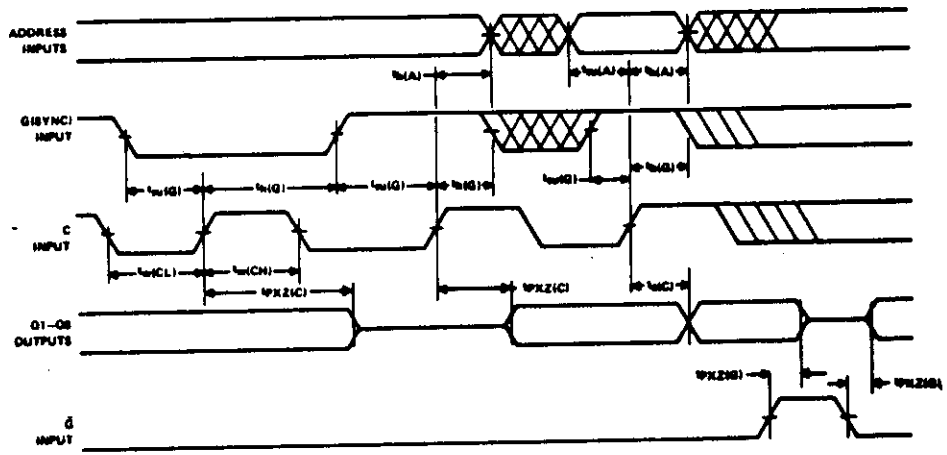


FIGURE 1 – SWITCHING WAVEFORMS FOR TYPES TBP28R45, TBP28R85, AND TBP28R166

recommended conditions for programming

PARAMETER		MIN	TYP	MAX	UNIT
Steady-state supply voltage, V_{CC}		4.5	5	5.5	V
Address input voltage	V_{IH}	2.4		5	V
	V_{IL}	0		0.5	
E3 and E4 input voltage (where appropriate)	V_{IH}	2.4		5	V
Voltage at all outputs except the one to be programmed		0		0.5	V
Supply voltage programming pulse (see Figure 2)	Voltage, $V_{CC(pr)}$	6.75	6	6.25	V
	Pulse width, t_w	1000		2000	μs
	Duty cycle		25	35	%
Select or enable programming pulse (see Figure 2)	Voltage, $V_{S(pr)}$	9.75	10	11	V
	V_{IL}				
Output programming pulse (see Figure 2)	Voltage, $V_{O(pr)}$	16.75	17	17.25	V
	Rise time, t_r	10		50	μs
	Pulse width, t_w	98	100	1000	μs
	V_{IL}	0		0.5	
Registered PROM verify clock pulse width	$t_{w(CH)}$		20		ns
Free-air temperature, T_A		0		55	°C

step-by-step programming instructions (see Figure 2)

1. Address the word to be programmed, apply 5V ± 10% to V_{CC} and active levels to all chip select (S and $\overline{S}$) or chip enable (E and $\overline{E}$) inputs.
2. Verify the status of a bit location by checking the output level. For registered PROMs a clock must be applied to the clock pin to verify the output level.
3. Increase V_{CC} to $V_{CC(pr)}$ with a minimum current capability of 200 milliamperes.
4. Apply $V_{S(pr)}$ to all the $\overline{S}$, $\overline{E}$ or $\overline{G}$ inputs. $I_I \leq 15$ mA.
5. Connect all outputs, except the one to be programmed, to a logic low level ($0 \leq V_{IL} \leq 0.5$ V). Only one bit is programmed at a time.
6. Apply the output programming pulse for at least 98 microseconds. Minimum current capability of the programming supply should be 200 milliamperes.
7. After terminating the output pulse, disconnect all outputs from V_{IL} conditions.
8. Reduce the voltage at $\overline{S}$, $\overline{E}$ or $\overline{G}$ inputs to V_{IL}.
9. Reduce V_{CC} to steady-state voltage and verify output status. Note that for registered PROMs, a clock must be applied to the clock input pin to verify output status.
10. Repeat steps 3 through 9 for each bit location that requires programming.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts. Note that registered PROMs must be clocked to verify the output condition.

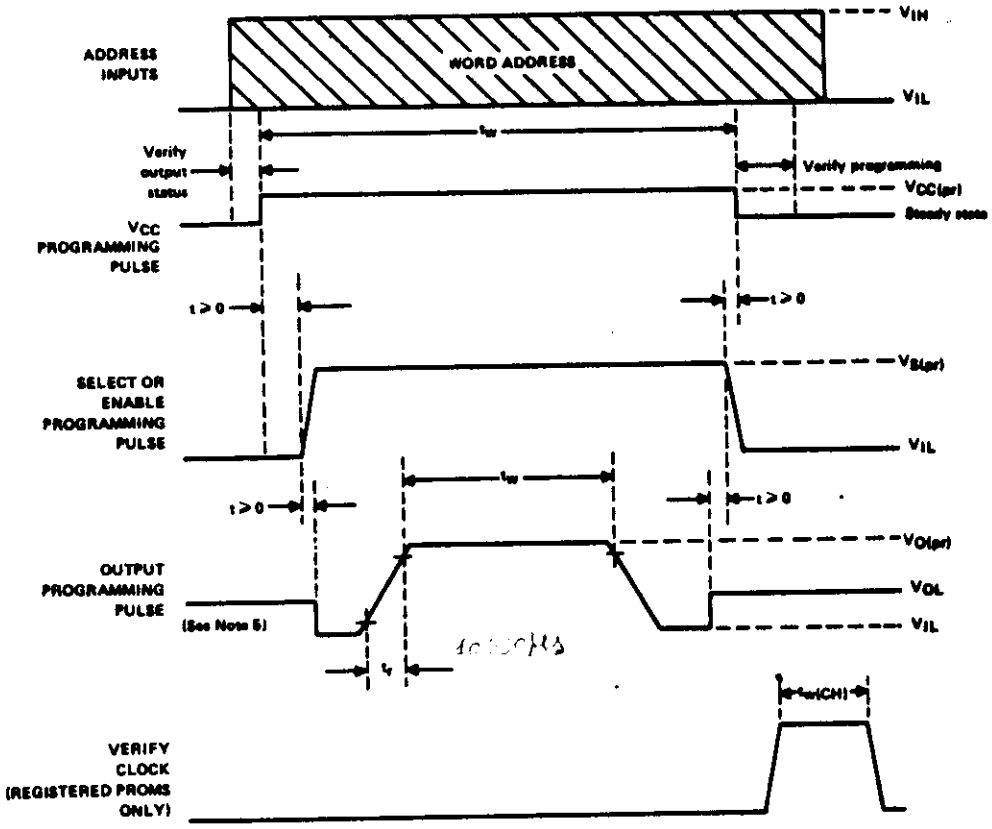


FIGURE 2 – TIMING DIAGRAM AND VOLTAGE WAVEFORMS FOR PROGRAMMING SEQUENCE

NOTE: The output to be programmed may be forced to zero volts after the transition to $V_{O(pr)}$ at the E input has begun.